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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001
23995	7590	01/14/2008	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			MONDT, JOHANNES P	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/743,104	Applicant(s) OGIHARA ET AL.	
	Examiner Johannes P. Mondt	Art Unit 3663	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11/02/07, 12/05/07.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2,5,6,9,10,18,20,37 and 38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2,5,6,9,10,18,20,37 and 38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/05/07</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Amendment*

Amendment filed 11/02/07 forms the basis for this office action. In said Amendment applicants substantially amended the (only) independent claim 5 and added new claims 37 and 38. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

### *Information Disclosure Statement*

The examiner has considered the items listed in the Information Disclosure Statement filed on 11/02/07 with said Amendment. A signed copy of Form PTO-1449 is herewith enclosed.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claim 38** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitations "an entire portion of the planarized film is directly disposed on an upper surface of said planarized region" and "an entire lower surface of the planarized film contacts the upper surface of said planarized region" are not supported by the original specification including original claims. The

details of the planarized film are only disclosed with reference to what reasonably must be interpreted as portions not necessarily including the "entire portion" and "entire lower surface". Therefore, said limitations constitute new matter.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 2, 5-6, 9-10, 18, 20 and 37-38** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "a flatness of a planarized region" in the independent claim 5, line 7, is poly-interpretable: see, e.g., Hendron et al (US 2002/008943 A1), in which two alternative definitions of semiconductor wafer flatness are summarized, namely: peak-to-valley flatness and RMS [measurement of] flatness. Therefore, the claims are indefinite.

5. **Claim 38** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "entire portion" is a contradiction in terms: portion being a part, and entire being the whole. Therefore, the meets and bounds of claim 38 are not defined.

6. **Claim 38** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitations "an entire portion of the planarized film is directly disposed on an upper surface of said planarized region" and "an entire lower surface of the planarized film contacts the upper surface of said planarized region",

being unsupported by the specification as originally filed, lack, because of said lack of support, the necessary well-defined meets and bounds, and hence claim 38 is indefinite.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. ***Claims 2, 5-6, 9-10, 18 and 38*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Konuma et al (US 2001/0019133 A1) (previously cited) in view of Blalock et al (US 2002/0187650 A1). N.B.: The rejection is offered subject to the noted indefiniteness under 35 USC 112, second paragraph (see section 4 in this Office Action), assuming that no distinction between "flatness" as disclosed in the art of semiconductor wafer passivation and as disclosed in the specification needs to be made.

*On independent claim 5: Konuma et al teach a combined semiconductor apparatus ([0009]-[0024], [0043]-[0251] and Figures 1-14; specifically also title and abstract: both control of current and light-emitting components being comprised in said apparatus), comprising:*

a silicon substrate 11/38 ([0044] for 11, [0013] for 38: note that i-Si is included in the embodiments of passivation film 38) having an integrated circuit formed therein (thin film transistors (TFTs) 201 and 202: see [0049]-[0057]), the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit (wiring pattern comprising source and drain electrodes 21, 22, 36 and 37 of said thin film transistors 201 and 202, e.g.);

a planarized region (the portion of 39 (see [0014]) within the lateral extent of EL device 203: see [0056]) defined over said rough or irregular surface of said silicon substrate;

a thin film (either 40, 40/41a/41b, or a portion of 40, e.g., the one with horizontal main surface (see [0063]-[0064] and [0068]-[0080] and Fig. 2) disposed over said planarized region; and

a semiconductor thin film 42 (see [0081]-[0082]) disposed over said thin film (N.B.: the recited organic materials are semiconductors: see, e.g., col. 15, l. 8-25 in Yamazaki et al (6,739,931 B2), cited here not for teaching at least in this respect not, but merely for recitation of fact),

the semiconductor thin film including a light-emitting element 42 (loc.cit.) and being bonded on said thin film 40, so that said semiconductor thin film is disposed above the integrated circuit and said thin film 40 electrically connects said light-emitting element to said integrated circuit (because 40 is a pixel electrode connected to drain wiring 37 of TFT 202 as well as abutting the EL layer 42 according to its function as pixel electrode), wherein:

said semiconductor thin film is made of a compound semiconductor as a main material (the recited organic semiconductor materials are also compounds); and

a surface of said thin film 40 on a side of said semiconductor thin film is made as planar as possible (being the surface on which the EL layer 42 is formed) (see [0014]).

Therefore, said thin film 40 meets the limitation "planarized film" as well.

In this regard it is noted that the limitations "planarized" (claim 5, lines 6, 8 (twice), 9, 11, 13 and 17) and "has been subjected to a planarizing process" (final line of claim 5) constitute product-by-process limitations and are only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting the final structure, are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the

product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113.

Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the relevant layers have been made to be as planar as possible (see above) and hence the limitations are met to the extent impacting on the final structure.

*Konuma et al do not necessarily teach* the limitation "a flatness of the planarized region being not more than 10 nanometers.

*However, it would have been obvious to include said limitation in view of Blalock et al, who, in a published U.S. patent application drawn to semiconductor wafer planarization (see title, abstract, [0001]-[0019]), hence art analogous to the problem posed by the rough or irregular surface that Konuma et al solve through planarization, teach that a planarized region over a semiconductor wafer with a rough or irregular surface can achieved such that the flatness of said planarized region is not more than 10 nanometers (see par. [0036]). It is an obvious objective in the art of planarization to create maximal surface flatness; following the planarization technique by Blalock et al a surface flatness of not more than 3 to 3.5 nm, hence meeting the claim limitation "not more than 10 nm", can be created. One of ordinary skill in the art when confronted with the invention by Konuma et al and the planarization of a rough or irregular semiconductor surface needed therein (see Konuma et al, par. [0014]) would have been led to the technique by Blalock et al drawn to planarization of semiconductor surfaces to at least the quantitative level as claimed. Motivation to include the teaching by Blalock in*

the invention by Konuma thus derives immediately from the good quality of flatness which is the objective of the planarization technique.

*On claim 2:* said planarized region formed by 39 is a part of said surface of said planarized silicon substrate 11/38 ([0061]). The limitation "which has been subjected to a planarizing process" constitutes a product-by-process limitation and hence is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting the final structure, are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al*, 218 USPQ 289, 292 (Fed. Cir. 1983), and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the relevant layer has been made to be planar and hence the limitations are met to the extent impacting on the final structure.

*On claim 6:* said planarized film includes an electrically conductive layer contacting with said light-emitting element (pixel electrode 40); and an inter-dielectric layer formed in a region peripheral to said electrically conductive layer (41a, 41b) (see [0068]-[0080]) (N.B.: protective layer 41 abuts pixel electrode 40, and hence the thin film may be

defined to be 40/41a/41b, which is planarized in a sub-region, hence meets the limitation 'planarized film').

*On claim 9:* said semiconductor film 42 has a common electrode layer 43 on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor film (see common electrode 352 in Figure 12 and discussion, [0167], of an EL device with additional sealing structure but otherwise identical to the device of Figure 10, which is the device with pixel depicted in Figure 2, and hence element 352 is equivalent to electrode 43 therein), in which said light-emitting element is formed, and said second surface of said semiconductor thin film is disposed on a side (namely the upper side) of said planarized region of said silicon substrate.

*On claim 10:* said integrated circuit includes individual electrode terminals (source, drain electrode terminals and gate electrode terminals of both TFT 201 and TFT 202); and said apparatus further comprises individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual terminals (see Figure 10, interconnecting lines 612, 613 and 614, e.g.: see [0154]).

*On claim 18:* said light-emitting elements are a plurality of light-emitting elements arranged in said semiconductor thin film (Figures 3A and 3B, see [0043]).

*On claim 38:* this rejection is offered subject also to the noted indefiniteness under 35 USC 112, second paragraph, in section 5 above, assuming any portion as defined, even a subset thereof, e.g., portion with a horizontal main surface, such as in Figure 2 of Konuma et al. In addition, the claimed planarized film may be defined beforehand to

be a portion of a planarized film with horizontal main surface. An entire portion of the planarized film 40, namely: a portion with horizontal main surface, is directly disposed on an upper surface of said planarized region, and an entire lower surface of the planarized film contacts the upper surface of said planarized region, namely the entire horizontal lower surface thereof (see Fig. 2, e.g.).

10. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Konuma et al and Blalock et al as applied to claim 5, in view of Tsuruoka et al (JP 2001167874 A).

As detailed above, claim 5 is unpatentable over Konuma et al in view of Blalock et al. Konuma et al do not necessarily teach the further limitation defined by claim 20.

*However, it would have been obvious to include said further limitation in view of Tsuruoka et al, who, in a patent document on an organic electroluminescent element, hence analogous art, teach the application of said organic electroluminescent element as the light source of an optical printer head (see English Abstract and also Derwent Abstract). Motivation to include the teaching by Tsuruoka et al in the invention by Konuma et al at least derives from the benefit of high picture quality and low manufacturing cost, as explicitly stated by Tsuruoka et al (see English Abstract, as well as 'Advantage' in Derwent Abstract).*

### ***Response to Arguments***

11. Applicant's arguments filed 11/02/07 have been fully considered but they are not persuasive. In particular:

Applicant's traverse based on the newly introduced limitation as set forth on pages 7-8 is not persuasive, with reference to the rejection under 35 USC 103(a), which is herewith included by reference in response to said traverse.

Furthermore, applicant's argument that "there is no disclosure or suggestion that Konuma's protective portions 41a and 41b are planarized together with the pixel electrode 40" does not correspond to the actual claim language, which reads as follows: "a planarized region defined over said rough or irregular surface of said silicon substrate", where "said surface" is a rough or irregular surface *due to* at least a wiring pattern of the integrated circuit", while roughness or irregularity can be due to a wiring pattern even at an angle that is oblique with regard to the normal of the substrate. Even *arguendo*, what is planarized in Konuma et al is a step formed by a wiring pattern, namely: by the thin film transistors (TFTs): see paragraph [0014] as cited in the Office Action. See also [0013]. Therefore, the latter argument fails to persuade.

Applicant's argument that Tsuruoka et al is non-analogous art (pages 9-10 of Remarks) is not persuasive, because both Konuma et al and Tsuruoka et al are concerned with organic EL elements (see Konuma et al, paragraphs [0001]-[0024], and Tsuruoka et al, English Abstract), while, even *arguendo*, what needs to be learned from Tsuruoka et al merely is the application of organic EL technology to optical printer heads; While applicant is once again reminded of the semiconductor nature of the thin film 42 with reference to Yamazaki et al (6,739,931 B2) as recited for establishment of fact (rather than teaching) in the previous Office Action.

Finally, applicant's argument of patentability of newly added claims 37-38 as being based on allegedly allowable claims 5 and 6 fails to persuade because, as explained above, claims 5 and 6 are not allowable.

Said newly added claims 37 and 38 have been examined for the first and earliest possible time.

### ***Conclusion***

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 8:00 - 18:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM  
January 11, 2008

Primary Patent Examiner:

  
Johannes Mondt (Art Unit: 3663)